1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Power loss and thermal modeling
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6. Power loss and thermal modeling
1. Motivation: device thermal management importance

Two electrical parameters that are dependent on temperature

1. $R_{DS(on)}$ and conduction loss

$R_{DS(on)}$ Temperature Dependence

- $R_{DS(on)}$ vs $T_J$ for GS66508B

Need to properly manage $T_J$ to minimize losses

2. Transconductance and switching loss

Typical $I_{ds}$ vs. $V_{gs}$

- $T_J=25^\circ C$
- $T_J=150^\circ C$

Transconductance $g_m$ vs $T_J$ for GS66508B

- $T_J=25^\circ C$
- $T_J=75^\circ C$
- $T_J=125^\circ C$

GS66508 $E_{on}$ with $T_J$ variation

- $E_{on}@400V/20A/15ohm/25^\circ C=74\mu J$
- $E_{on}@400V/20A/15ohm/125^\circ C=122\mu J$
1. Motivation: device thermal management importance

Reasons to keep device cool:

1. Prevents thermal runaway at maximum/worst operating conditions

- Conduction Loss
- Switching Loss
- Thermal iteration
- \( R_{DS(on)} \)
- \( T_J \)
- \( g_m \)
- \( g_m \)
- \( R_{DS(on)} \)

Thermal runaway

Thermal steady-state

But also to:

2. Reduce overall loss and improve system efficiency

3. Improve system reliability

A good thermal design from both device-level and system-level is critical.
1. Motivation: device thermal management importance

A good thermal design also improves design power density

Example:

Compared to FR4 PCB heat transfer, the GaN Systems’ insulated metal substrate (IMS) design reduces the heatsink volume for high-power applications.

Simulation comparison of IMS vs FR4 PCB:

- Forced-air cooling, $T_A=25 \, ^\circ C$, same PCB size
- Keep $T_J=100 \, ^\circ C$. With power loss increasing, increase heatsink size to keep $T_J$ constant.
1. Motivation: device thermal management importance

2. Introduction of power loss and thermal basics
   2.1 Power loss
   2.2 Heat transfer, thermal resistance, and junction temperature

3. Bottom-cooled device thermal design consideration

4. Top-cooled device thermal design consideration

5. Device selection based upon thermal consideration

6. Loss and thermal modeling
2.1 Introduction of power loss mechanism

Switch device’s energy loss can be mainly summarized as three different types. Power loss is \( P = E \times F_{sw} \).

1. Hard-switching device energy loss trajectory
2. Synchronous-rectification device energy loss trajectory
3. ZVS soft-switching device energy loss trajectory

Power loss mechanisms under various operating conditions are well understood and characterized.

GS66508T switching loss @ 400V
GS66508T switching loss @ 200V
2.1 Introduction of power loss reduction by using GaN

**Switching method**

- **3. ZVS soft-switching mode**
  - Fast switching speed
  - Low energy-related $C_{oss(ER)}$
  - Low time-related $C_{oss(TR)}$
  - Low gate charge $Q_g$

- **1. Hard-switching mode**
  - Zero reverse recovery loss
  - Low capacitive $E_{oss}/E_{qoss}$ loss
  - Excellent transconductance

**GaN characteristics**

- Switching-off loss
- Inductive energy to achieve ZVS, less reactive power loss
- Deadtime
- Gate driver loss

**System impact**

- Due to its excellent electrical performance, GaN HEMT enhances both soft-switching and hard-switching applications

---

**System examples**

- 170 W PFC + LLC adapter
- 300 W PFC + LLC adapter
- 3 kW CCM Totem-pole PFC
- 10 kW Three-phase traction inverter
2.2. Heat transfer, thermal resistance, and junction temperature

Heat transfer occurs mainly in three different ways:

- **Conduction** – through direct contact
- **Convection** – through fluid movement (air is a fluid)
- **Radiation** – through electromagnetic waves

---

**Analogy between thermal and electrical parameters**

<table>
<thead>
<tr>
<th>Thermal parameters</th>
<th>Electrical parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature $T$ (°C)</td>
<td>Voltage $V$ (V)</td>
</tr>
<tr>
<td>Power $P$ (W)</td>
<td>Current $I$ (A)</td>
</tr>
<tr>
<td>Thermal resistance: $R_\theta$ (°C/W)</td>
<td>Resistance $R$ (Ω)</td>
</tr>
<tr>
<td>Thermal capacitance: $C_\theta$ (W·s/°C)</td>
<td>Capacitance $C$ (F)</td>
</tr>
</tbody>
</table>

$$\Delta V (V) = \Delta T (°C)$$

$$R (\Omega) = R_\theta (°C/W)$$

$$C (F) = C_\theta (W·s/°C)$$

$$I (A) = P (W)$$
2.2. Heat transfer and thermal resistance on GaN

Junction temperature calculation: \( T_J = T_A + P \times R_{0JA} \)

Excellent electrical performance (figure-of-merit) of GaN HEMTs limit the overall power loss

Beyond conventional “figure-of-merit” This presentation shows how to fully utilize GaN by thermal design to maximize the overall performance of GaN HEMTs
Application note outline

1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Loss and thermal modeling

Flip Chip: Low Inductance, low $R_{ON}$ Cu Pillars

Substrate Pad on Top

Substrate Pad tied to Source

Drain, Gate, Source on Bot (GaNPX® package)

Device structure with GaN PX®-T package
3. Top-cool design – Thermal interface material (TIM) selection

Thermal simulation operating Conditions:
- GS66516T is applied with 10 W power loss on it
- $T_{HS} = 25 \, ^\circ C$

<table>
<thead>
<tr>
<th>TIM Thickness (mm)</th>
<th>SIL-PAD K-4</th>
<th>SIL-PAD 1500ST</th>
<th>GAP3000S30</th>
<th>HI-FLOW 300P</th>
<th>GAPFILLER GS 3500S35-07</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.152</td>
<td>0.203</td>
<td>0.25</td>
<td>0.102</td>
<td>0.178</td>
</tr>
<tr>
<td>Thermal conductivity (W/m·K)</td>
<td>0.9</td>
<td>1.8</td>
<td>3.0</td>
<td>1.6</td>
<td>3.6</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Thermal Resistance (°C/W)</th>
<th>RTIM</th>
<th>RJC</th>
</tr>
</thead>
<tbody>
<tr>
<td>SIL-PAD K-4</td>
<td>4.12</td>
<td>0.35</td>
</tr>
<tr>
<td>SIL-PAD 1500ST</td>
<td>2.94</td>
<td>0.35</td>
</tr>
<tr>
<td>GAP3000S30</td>
<td>2.29</td>
<td>0.35</td>
</tr>
<tr>
<td>HI-FLOW 300P</td>
<td>1.84</td>
<td>0.35</td>
</tr>
<tr>
<td>Gapfiller GS 3500S35-07</td>
<td>1.49</td>
<td>0.35</td>
</tr>
</tbody>
</table>

Key parameters for TIM material selection: dielectric strength, mechanical strength, and cost.

3. Top-cool design – Mounting consideration

**Center mounting hole for small heatsink**

- Balanced pressure across 2 devices
- Typical recommended maximum pressure ~50psi.
- Tested up to 100psi without failure

**2 or more mounting holes for large heatsink**

- Excess PCB bending causes stress on SMD parts which should be avoided
- Locate mounting holes near to GaNPX®-T package
- If warranted, use a supporting clamp bar on top of PCB for additional mechanical support, not common
3. Top-cool design – Voltage isolation clearance

When using a heatsink, design to meet the regulatory creepage and clearance requirements

- Use TIM to cover Heatsink edge in areas where clearances must meet Standards

- Avoid placing Through Hole Components near GaNPX®-T package

- Use Pedestal Heatsink design to increase clearances and allow for placement of SMT components under the heatsink

A pedestal heatsink provides clearance beneath the heatsink for the placement of other SMT devices

Ensure the air gap here meets the safety clearance standards of your design

Ensure both creepage and clearance meets the safety standards

A pedestal heatsink provides clearance beneath the heatsink for the placement of other SMT devices

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Ensure both creepage and clearance meets the safety standards

A pedestal heatsink provides clearance beneath the heatsink for the placement of other SMT devices
### 3. Top-cool design – Package bending pressure and deformation

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Deformation Safe Limit (µm)</th>
<th>Pressure Safe Limit (PSI)</th>
</tr>
</thead>
<tbody>
<tr>
<td>GS66508T</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>GS66516T</td>
<td>120</td>
<td>100</td>
</tr>
</tbody>
</table>

**Diagram:**
- **Deformation Test**
  - Top view: GaNPX®-T package
  - Side view: GaNPX®-T package
  - Loading
  - Deformation
- **Pressure Test**
  - Loading
  - Solder joints
  - GaNPX®-T package
  - PCB
  - Side view
DUT subject to 100 PSI over 3 pulses, with no shift in Leakage Currents

400 volts $V_{DS}$ applied to each DUT (@ 25°C)

Leakage Current = $I_{DSS} + I_{GS} + I_{BULK}^*$ (*Substrate)
3. Top-cool design – Thermal resistance measurement

1. The measured $R_{\text{thJHS}}$ and $R_{\text{thJA}}$ for GS66516T are 3 °C/W and 4.2 °C/W, respectively.

2. GS66516T can dissipate 29 W loss per device.

Heat sink size: 3.4x3.4x2.5 cm³
Fan flow rate: 3.3 m³/min
Tested GS66516T-based evaluation board
TIM: Sil-Pad 1500ST

Inside setup box region

Top-cool force-air cooling thermal Resistance test setup

$y = 4.2472x + 21$
1. Motivation: device thermal management importance

2. Introduction of power loss and thermal basics

3. Top-cooled device thermal design consideration

4. Bottom-cooled device thermal design consideration
   4.1 FR4 PCB Bottom-cool design
   4.2 IMS Bottom-cool design

5. Device selection based upon thermal consideration

6. Loss and thermal modeling
FR4 PCB and IMS for bottom-cooling are both suitable solutions. Customer selection depends on design trade-off.

Performance comparison of 2 thermal design options for bottom-cool devices:

- **FR4 PCB Cooling with Vias**
  - Thermal resistance: Good
  - Electrical Insulation: Use TIM
  - Cost: Lowest
  - Advantages: Standard process, Layout flexibility
  - Design challenges: High PCB thermal resistance

- **Insulated Metal Substrate (IMS)**
  - Thermal resistance: Best
  - Electrical Insulation: Yes
  - Cost: Low
  - Advantages: Electrically isolated
  - Design challenges: Usually layout limited to 1 layer, Parasitic inductance, Coupling capacitances to the metal substrate
4.1. FR4 PCB Bottom-cool design – PCB thermal design

Thermal vias design

- GS66508B with device power loss 10 W. 4 layers copper with 2 oz (70 µm) copper thickness. \( T_{HS} = 25 ^\circ C \)
- Thermal via setup: 0.3 mm diameter with 0.64 mm pitch. Standard 25 µm copper plating thickness. No via filling.

\[ R_{\theta JHS} = 14.1 ^\circ C/W \]
\[ R_{\theta JHS} = 8.8 ^\circ C/W \]
\[ R_{\theta IHS} = 8.1 ^\circ C/W \]

- Place thermal vias fully under the device thermal pad to maximize effectiveness
- Thermal via area is extendable based upon PCB design area

![Thermal Vias Diagram](image)
4.1. FR4 PCB Bottom-cool design – PCB thermal design

Number of copper layers and copper thickness

- GS66508B with device power loss 10 W. $T_{HS} = 25 \, ^\circ C$. Overall PCB thickness keeps the same (1.6mm).
- With 55 thermal vias as example.

Increase in copper layer and copper thickness reduces $R_{\theta}$ further, with the PCB cost as the trade-off.
4.2. IMS Bottom-cool design

IMS I
- Designed for high power application (3~12kW).
- Applied GaN HEMT: GS66516B single, or 2x, 4x paralleling

IMS II
- Compact. Designed for mid-high power application (1~3kW).
- Applied GaN HEMT: single GS66508B or GS66516B

IMS improves power density for high-power applications
4.2. IMS Bottom-cool design – Solder voids consideration

Operating conditions: $P = 7.98\ W$, $T_{\text{IMS}} = 85\ ^\circ\text{C}$, GS66508B is applied

No voids under the package: $R_{\theta\text{JIMS}} = 2.18\ ^\circ\text{C/W}$

32% voids under the package: $R_{\theta\text{JIMS}} = 3.16\ ^\circ\text{C/W}$

Measurement and Xray results

Limit voids to achieve the best IMS thermal performance

Operating temperature: $T_J = 102.43\ ^\circ\text{C}$

Experimental results with the device with voids

Xray results on a device with voids
1. The $R_{\theta JA}$ for GS66516B based IMS is 2.9 °C/W.
2. GS66516B can dissipate 43 W loss per device.
1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Loss and thermal modeling
5. Device selection from thermal consideration – single device

- **FR4 PCB** (*R*\textsubscript{θHSA}=1.25 °C/W*)
- **FR4 PCB** (*R*\textsubscript{θHSA}=1.25 °C/W*)
- **Top-cool** (*R*\textsubscript{θHSA}=1.25 °C/W*)
- **IMS** (*R*\textsubscript{θHSA}=1.5 °C/W*)

**Device performance and its thermal solution define the system max power**

**Higher power applications with higher device loss?**

1. Better cooling design: Better heatsink design, better fan, liquid cool, DBC substrate, etc.
2. Larger GaN transistor
3. Parallel GaN transistors

---

* *R*\textsubscript{θHSA} =1.25 °C/W*
** *R*\textsubscript{θHSA} =1.5 °C/W**

---

**Measured device power loss vs *T*\textsubscript{j} with different cooling methods – single discrete device solution**

---

---
5.2 Enhance thermal performance by paralleling

Paralleling GaN is a proven technique to increase system power

Parallelizing reduces both system $R_{DS(on)}$ (electrical) and $R_\theta$ (thermal)

Example:

- 4xGS66516B parallel to share 136 A load current with hard-switching on/off.
- Randomly selected transistors.
- $T_J$ difference is $<6$ °C for the worst case.

![Thermal network comparison](image)

- 4xGS66516B parallel to share 136 A load current with hard-switching on/off.
- Randomly selected transistors.
- $T_J$ difference is $<6$ °C for the worst case.
5. **Device selection from thermal consideration - including parallel**

- **Device performance and its thermal solution define the max system power**
- **By reducing both loss and thermal resistance, paralleling makes GaN achieve higher power**

- **Device loss vs TJ with different cooling methods including parallel solution**
1. Motivation: device thermal management importance
2. Introduction of power loss and thermal basics
3. Top-cooled device thermal design consideration
4. Bottom-cooled device thermal design consideration
5. Device selection based upon thermal consideration
6. Loss and thermal modeling
   6.1 SPICE modeling
   6.2 PLECS modeling
6.1. SPICE modeling

GaN Systems provides a two-level SPICE model. For thermal modeling, use L3 model.

### Definitions of model levels

<table>
<thead>
<tr>
<th>Suffix</th>
<th>Level</th>
<th>Terminals</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>_L1</td>
<td>1</td>
<td>G, D, S, SS (if applicable)</td>
<td>General electrical simulations on application/converter level circuits. Focus on simulation speed.</td>
</tr>
<tr>
<td>_L3</td>
<td>3</td>
<td>G, D, S, SS (if applicable), Tc, Tj</td>
<td>In addition to L1, L3 also includes the thermal model and package stray inductance.</td>
</tr>
</tbody>
</table>

### Functions of model levels

<table>
<thead>
<tr>
<th>Functions</th>
<th>Level 1</th>
<th>Level 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>IV performance as a function of temperature</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Voltage-dependent capacitance</td>
<td>✓</td>
<td>✓</td>
</tr>
<tr>
<td>Thermal model</td>
<td>×</td>
<td>✓</td>
</tr>
<tr>
<td>Package stray inductance</td>
<td>×</td>
<td>✓</td>
</tr>
</tbody>
</table>

Inside the SPICE model

- **L1 device symbol**
  - D
  - G
  - S
  - SS

- **L3 device symbol**
  - D
  - G
  - S
  - SS
  - Tc
  - Tj

Modeled parasitic inductance in L3

- **L_g**
- **L_d**
- **L_s**
- **L_ss (if applicable)**
6.1. SPICE modeling

Junction-to-case thermal modeling

4-stage Cauer RC thermal model to accurately represent device

Cauer model is applied for junction-to-case thermal modeling due to:
1. Unlike the Foster model (curve-fitting model), Cauer RC network is based on the physical property and packaging structure.
2. The RC elements are assigned to the package layers.

<table>
<thead>
<tr>
<th></th>
<th>$R_\theta$ (°C/W)</th>
<th>$C_\theta$ (W·s/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>#1</td>
<td>0.015</td>
<td>8.0E-05</td>
</tr>
<tr>
<td>#2</td>
<td>0.23</td>
<td>7.4E-04</td>
</tr>
<tr>
<td>#3</td>
<td>0.24</td>
<td>6.5E-03</td>
</tr>
<tr>
<td>#4</td>
<td>0.015</td>
<td>2.0E-03</td>
</tr>
</tbody>
</table>

Example: GS66508B $R_{\theta JC}$ modeling

GS66508B Cauer RC model parameters
6.1. SPICE modeling

**T<sub>J</sub>** pin can be used as an input or output, depends on the simulation purpose.

GAN SYSTEMS SWITCHING LOSS DOUBLE PULSE TEST BENCH

- Set **T<sub>J</sub>** pin to a constant value as an input to check the **E<sub>on</sub>/E<sub>off** at the desired **T<sub>J</sub>**.

- **T<sub>J</sub>** pin can be used as an input or output, depending on the simulation purpose.

- Set **T<sub>J</sub>** pin as output to check **T<sub>J</sub>** in both steady-state and transient.

Continuous Converter Simulation

- **P<sub>SW** = **V<sub>DS** * **I<sub>D**
- **E<sub>ON** = 106uJ
- **E<sub>OFF** = 8uJ
6.2. PLECS modeling

Device-level simulation
(LTspice and Pspice)

- Device characteristics ($Q_g$, $C_{oss}/C_{iss}$, IV/CV curve, $E_{on}/E_{off}$)
- Simple system simulation (double-pulse test, buck, boost, etc.)
- See parasitic effect on switching performance

Converter/system-level simulation
(PLECS)

- Simplify the switching transient
- Observe converter operating waveforms
- Can handle complicated device-based system-level simulation/analysis

LTSPICE, PSPICE, and PLECS models assist system design to maximize performance
6.2. PLECS modeling

Switching loss modeling

- An $E_{\text{on}}/E_{\text{off}}$ scaling method is developed by GaN Systems.
- $E_{\text{on}}/E_{\text{off}}$ data can be scaled to different $T_J$, $V_{ds}$, and $R_g$.

Conduction loss modeling

- Deadtime loss modeling:

$$v_{gm}(I,T,V_{ds},R_{g-on},R_{g-off},g) = v(i<0) * (1-g) * (1.3-v_{g-off})$$

Thermal modeling (junction-to-case)

$R_g$-dependent equation:

$$E_{\text{on}}(v_i,T,E,R_{g-on},R_{g-off},g) = \frac{((R_{g-on}-10)^*v_i^2)/2}{(18.68+2.2e-9/(I_{24.4}/(1.3+I_{24.4})))/(6.13-I_{24.4})+E_{\text{on}}}$$
6.2. PLECS modeling verification

Based on GS66508
F_{sw}=200 \text{ kHz},
V_{in}=400 \text{ V},
V_o=193 \text{ V}
R_{\theta CA}=4.5 ^\circ \text{C/W}
6.2. PLECS modeling – System loss and thermal analysis

Example: UPS system

Bridgeless PFC

Isolated DC/DC

Single-phase inverter

PLECS model can be used for system-level analysis
GaN Systems also provide online simulation tool based on PLECS model

Welcome to the GaN Systems Circuit Simulation Tools

The Circuit Simulation Tool allows you to compare application conditions by implementing specific operating values. Choose various source and load parameters, number of devices to parallel, heat sink parameters etc. Live simulated operating and switching waveforms are generated as well as data tables showing calculations for loss and junction temperature allowing you to compare the effect of parameter variations or the operation of different parts directly.

You may also download the PLECS device model files for GaN Systems’ transistors.

- BRIDGELESS TOTEM-POLE PFC
- SINGLE-PHASE, 2-LEVEL INVERTER
- SINGLE-PHASE, 3-LEVEL HALF-BRIDGE INVERTER
- SINGLE-PHASE T-TYPE 3-LEVEL INVERTER
- ISOLATED HALF-BRIDGE LLC CONVERTER
- ISOLATED PHASE-SHIFT FULL BRIDGE CONVERTER
- THREE-PHASE TRACTION INVERTER
- DUAL ACTIVE BRIDGE

GaN PLECS model for both 100V and 650V device

All GaN Systems’ device models and 8 topologies are available online https://gansystems.com/design-center/circuit-simulation-tools/
Conclusions

• Good thermal design improves GaN transistor and system performance.

• Maximizing electrical and thermal design of GaN-based systems increases performance in soft-switching to hard-switching applications and operates efficiently from several watts to many kilowatts.

Key design tips provided in this app note

• Top-cool thermal design: TIM and heat sink mounting

• Bottom-cool thermal design: PCB design and solder voids

• Device selection including paralleling options

• Modeling tools to assist with power loss calculation and thermal design


Join the wave - revolutionize your power electronics

**Broatest line of Products**

**650 V GaN**
- GS66502B
  - 7.5 A, 200 mΩ
  - 6.6 x 5.0 mm
- GS66504B
  - 15 A, 100 mΩ
  - 6.6 x 5.0 mm
- GS66506T
  - 22 A, 67 mΩ
  - 5.6 x 4.5 mm
- GS66508T
  - 30 A, 50 mΩ
  - 7.0 x 4.5 mm

**100 V GaN**
- GS61004B
  - 45 A, 15 mΩ
  - 4.6 x 4.4 mm
- GS61008P
  - 90 A, 7 mΩ
  - 7.6 x 4.6 mm
- GS61008T
  - 90 A, 7 mΩ
  - 7.0 x 4.0 mm

**Many Eval Kits & Reference Designs**

**Half bridge power stage**
- EZDrive™ Eval Kit
- 650 V test kit

**High power Paralleling**
- 1.5 kW bridgeless totem pole PFC
- High density PFC/LLC

**3 kW bridgeless totem pole PFC**
- 300 W wireless power transfer

Class D Amp+SMPS Eval Boards

Learn more at gansystems.com